4. (Amended) Apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set.

5. (Amended) Apparatus as claimed in claim 1, wherein said processor core fetches instructions from an instruction address within said memory specified by a program counter value held by said processor core.

7. (Amended) Apparatus as claimed in claim 5, wherein, when an instruction of said second instruction set is executed, said program counter value is advanced to specify a next instruction of said second instruction set to be executed.

8. (Amended) Apparatus as claimed in claim 5, wherein said program counter value is saved if an interrupt occurs when executing instructions of said second instruction set so and is used to restart execution of said instructions of said second instruction set after said interrupt.

9. (Amended) Apparatus as claimed in claim 1, wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack.

10. (Amended) Apparatus as claimed in claim 1, wherein said processor has a register bank containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers.

12. (Amended) Apparatus as claimed in claim 9, wherein said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said stack, said instruction translator being operable to move between mapping states in dependence upon operations that add or remove stack operands held within said stack.

13. (Amended) Apparatus as claimed in claim 1, further comprising a bypass path within said instruction pipeline such that said instruction translator may be bypassed when instructions of said second instruction set are not being processed.

14. (Amended) Apparatus as claimed in claim 1, wherein said instructions of said second instruction set are Java Virtual Machine bytecodes.

19. (Amended) Apparatus as claimed in claim 17, wherein said fetch stage includes a plurality of multiplexers for selecting a variable length instruction from one or more of said current instruction word and said next instruction word.

20. (Amended) Apparatus as claimed in claim 17, wherein said instructions of said second instruction set are Java Virtual Machine bytecodes.

21. (Amended) Apparatus as claimed in claim 17, further comprising a bypass path within said instruction pipeline such that said instruction translator may be bypassed when instructions of said second instruction set are not being processed.

22. (Amended) Apparatus as claimed in claim 17, wherein

(i) at least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core; and

(ii) said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation.